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Covering the Period 15 July through 31 August 2009

POWER MEMS DEVELOPMENT

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Submitted in accordance with Deliverable A001 - Monthly Technical and Financial
SRI Project P19063

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ACTIVITIES AND PROGRESS

MEMS RESETTABLE CIRCUIT BREAKER (TASK 1.1)

Contributors: Susana Stillwell, Sunny Kedia, and Weidong Wang

Deliverable: 10 prototype packed MEMS-based resettable circuit breakers for testing and analysis in ONR laboratories.

Progress:

During this period, we developed a first revision of a process flow for the resettable circuit breaker. This process flow incorporates two wafers, one silicon (Si) and one silicon-on-insulator (SOI). The process flow will use wafer-to-wafer bonding and through-wafer etching to form a cantilever structure.

We also generated a test plan, and the first iteration mask design is in process based on the process flow. The concept of a MEMS resettable circuit breaker is that a MEMS cantilever will be pulled toward the bottom electrode by electrostatic actuation. The MEMS cantilever also has a thermal heater as shown in the solid model in Figure 1. As the current passes a threshold level, the thermal forces overcome the electrostatic actuation force, thereby disconnecting the circuit. Structure silicon of the silicon on insulator (SOI) wafer is selected as cantilever material (due to its low stress properties). Nichorme or platinum is the heater material. The bonding area, trace area, and electrostatic electrode consist of chrome/ gold.

MEMS SWITCH FOR DC-DC VOLTAGE CONVERTERS (TASK 1.2)

Contributors: Sunny Kedia, Shinzo Onishi and Scott Samson

Deliverable: Functional MEMS-based DC-DC convertor in a vacuum package

Progress:

During this month, implementation, modeling, layout, and process development for the device fabrication was initiated. The project goal is to deliver converters capable of converting 1.5 V battery power to 12 VDC at 10 µA with less than 10% ripple. The device operates similar to a Cockroft-Walton (CW) voltage multiplier, but replaces the traditional diodes with MEMS switches to increase efficiency. A simplified non-self-oscillating switch design and multiplier will be implemented later on. This approach will allow

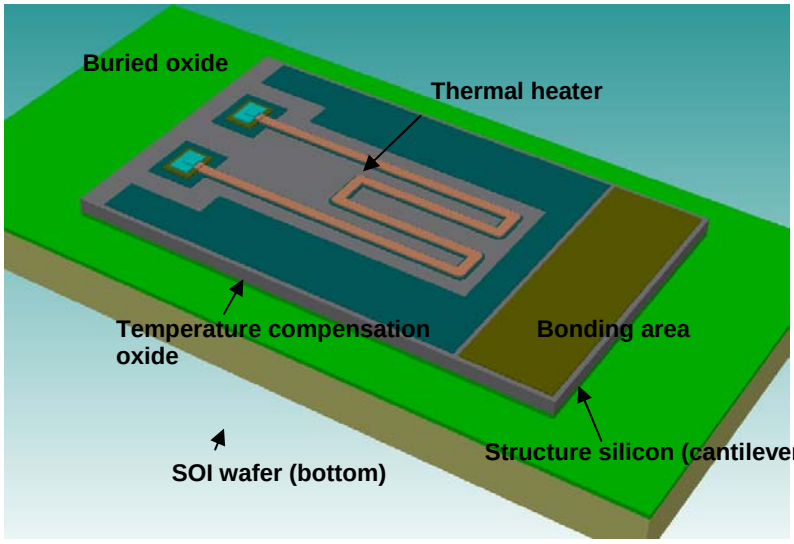


Figure 1. Coventorware solid model of SOI wafer illustrating the MEMS circuit breaker design

testing of the MEMS device's electromechanical behavior, switch contact resistance and reliability, and converter performance using external low-voltage drive signals.

Analytical expressions[1] can be used to estimate pull-in voltage (V_{PI}) based on cantilever dimensions (width [w], thickness [h], air gap [d_o] and the material's Young's modulus [E]).

$$V_{PI} = \sqrt{\frac{2 E h^3 d_o}{8.37 \varepsilon l^4 \left(\frac{5}{6 d_o^2} + \frac{0.19}{d_o^{1.25} w^{0.75}} + \frac{0.19}{d_o^{1.25} l^{0.75}} + \frac{0.4 h^{0.5}}{d_o^{1.5} w} \right)}}$$

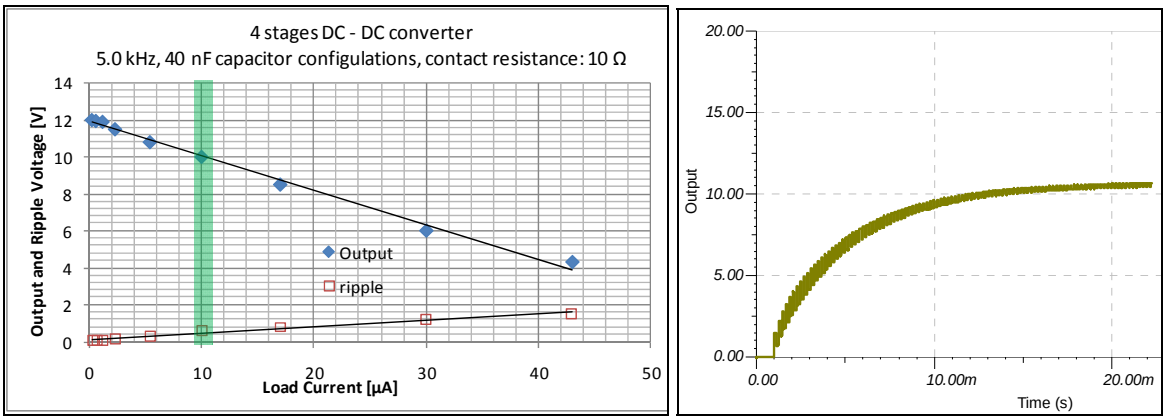
An integrated process flow has been developed. Much of the process is similar to the circuit breaker task. Based on prior experience, single crystal silicon and SOI wafers are being used to reduce risk of excessive cantilever curvature affecting performance. Device dimensions yielding switching closure near 1.5 V are being designed into a mask set. We are including in the design geometric design variations around the target operating point, as well as test structures, to account for and to measure variations in actual performance. The mask set is expected to be completed and received in early September.

The performance of a four-stage CW converter, which converts 1.5 VDC to 12V DC, was simulated using a *SPICE* simulation software package. We varied load conditions, switching frequency, and capacitance values, and included a moderately high 10 ohm contact resistance in some simulations. The effect of contact resistance of 10 ohms for the targeted 10 µA (and higher) load was found to be insignificant. Voltage droop under higher loads was found to be much more significant than ripple (see Figure 2a). The Thevinin's equivalent circuit for the four-stage converter was found to be a 12 V supply with output resistance of

$$R = \frac{42.2}{C \times f} \text{ [ohms]}$$

where C is the capacitance value [F], and f is the switch operating frequency [Hz]. For less than 10% voltage droop with a 10 µA load and 5 kHz switch operating frequency, the integrated capacitors must be at least 70 nF, which are available in 0201 (0.6 mm x 0.3 mm) surface mount packages. In the first experiments, we will use 0201 capacitors instead of monolithically integrated capacitors. Upon turn-on, the output voltage stabilizes within 20 ms (see Figure 2b).

[1] S Chowdhury, M Ahmadi and WC Miller, "A closed-form model for the pull-in voltage of electrostatically actuated cantilever beams," J. Micromech. Microeng. v. 15, p. 756–763 (2005).



(a) (b)

Figure 2. Four-stage switch-based Cockroft-Walton (CW) voltage multiplier. (a) SPICE simulation results showing output voltage droop and ripple versus load current (green highlight denotes target load). (b) Startup output voltage for circuit with 70 nF capacitor, 5 kHz switch operating frequency and 10 µA load current.

DIAMOND HEAT SPREADER OR HEAT SINK FOR HIGH POWER MEMS SWITCHES APPLICATIONS (TASK 1.3)

Contributors: Priscila Spagnol, Shinzo Onishi, Drew Hanser, John Bumgarner

Deliverable: In this task we will deliver a prototype device fabricated on a thin-film diamond heat spreader layer and individual samples of diamond on Si or other suitable substrates for material evaluation.

Progress:

During this reporting period we defined the experimental plan to meet the deliverables and generated the list of tasks and milestones per period.

We also initiated a competitive analysis and literature search. Companies that sell diamond wafers were identified, and wafers will be purchased to serve as comparison to the ones we develop in house.

To achieve the deliverables, the main characteristic that needs to be evaluated is the diamond thermal conductivity. CVD diamond is clearly one of the most difficult materials to characterize thermally, not only because of its extreme high conductivity (κ) /diffusivity (D), but also its columnar microstructure and the resulting inhomogeneity, which creates a gradient in the local conductivity. The gradient depends on the direction of heat flow, i.e., the gradient is different for parallel or perpendicular, resulting in a pronounced anisotropy in the local conductivity. Some measurement techniques are more sensitive to this gradient and anisotropy than others. Many different techniques have been used to measure κ and/or D for CVD diamond. For this study we selected the 3 ω method (Figure 3), which uses harmonic Joule heating. A metal resistor, which is deposited on the surface of a dielectric film and serves as a heater, is supplied with a harmonic current to induce Joule heating. The temperature response of the sample is then calculated from the heater's resistance, which is found by measuring the third

harmonic of the heater's voltage using lock-in direction. This method, with a simple sample preparation, involves using different heater widths in order to vary the sensitivity to the anisotropy in the film. The benefit of this approach is that the in-plane and out-of-plane thermal conductivity can be measured from one device structure and the same setup, instead of being measured separately.

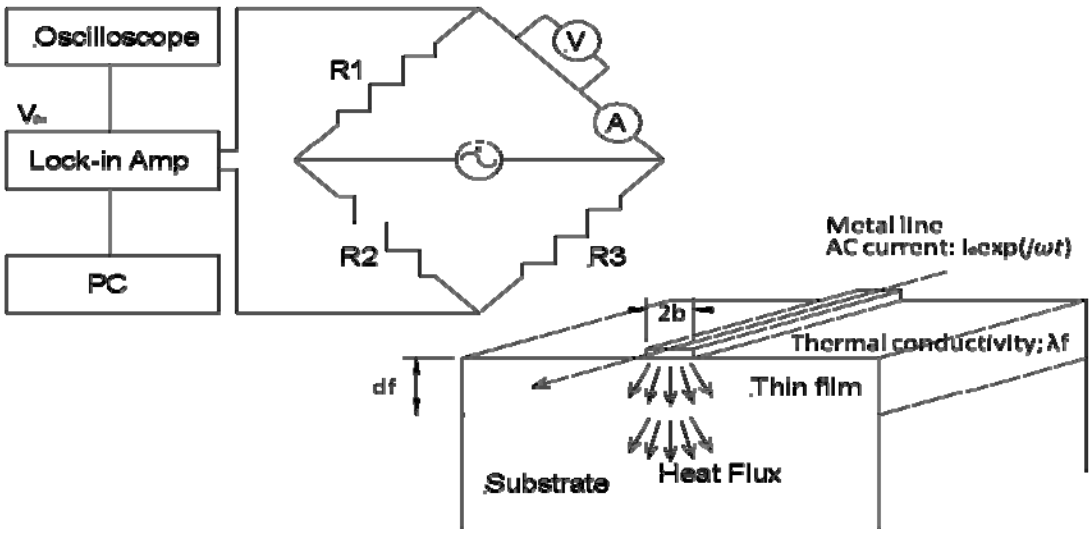


Figure 3. 3 ω method diagram

In parallel, we have been depositing diamond samples because it requires such a long run (5-7 days) to grow free-standing films. We used Si (100) 2" diameter x 3mm thick substrates and deposited 2.0 μm of thermal SiO_2. The wafers were than ultrasonicated in a nanodiamond water suspension for 20 min and cleaned in methanol for more than 10 min. The nanocrystalline deposition conditions were:

Sample	Temp (^oC)	H_2 (sccm)	CH_4 (sccm)	O_2 (sccm)	Pressure (Torr)	Power (kW)	Dep. time
NCD	700	254	45	0.6	30	1.0	6h to 27.2h

Figure 4 is a scanning electron microscopy (SEM) image of the nanocrystalline diamond (NCD) film. After the NCD deposition, the stage was changed from heated to cooled and microcrystalline diamond (MCD) film started to be deposited on the previous films to fabricate the free standing diamond film.

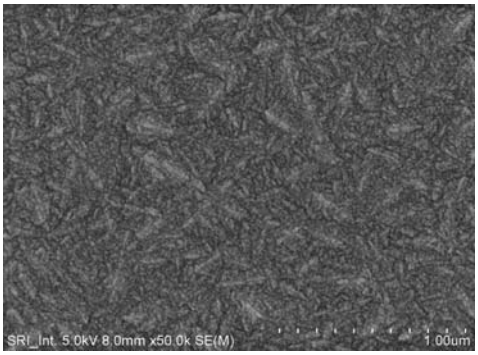


Figure 4. SEM image of NCD film. Similar images were obtained for all the deposition conditions.

POSITRON TRAPPING AND STORAGE (TASK 2)

Contributors: Ashish Chaudhary, Friso van Amerom, Tim Short

Deliverable: A minimum of 4 MEMS-based trap structures for RF trapping of electrons

Progress:

Below we list the main accomplishments on this task.

1. We conducted preliminary simulations and literature reviews, which indicate that linear traps are more suitable to trap electrons than cylindrical traps due to ease of injection of electrons.
2. We developed a concept of surface electrode type linear trap.
3. We performed modeling in SIMION 3-D ion optics software to investigate the electron trapping capability of various shapes of surface electrode-type linear traps (see Figure 5).
4. We determined key device design parameters including scale, RF frequency, and voltage.
5. We identified critical challenges and reviewed literature for electron injection, cooling and detection methods.
6. We identified the major components required to build a test setup for an electron trap.

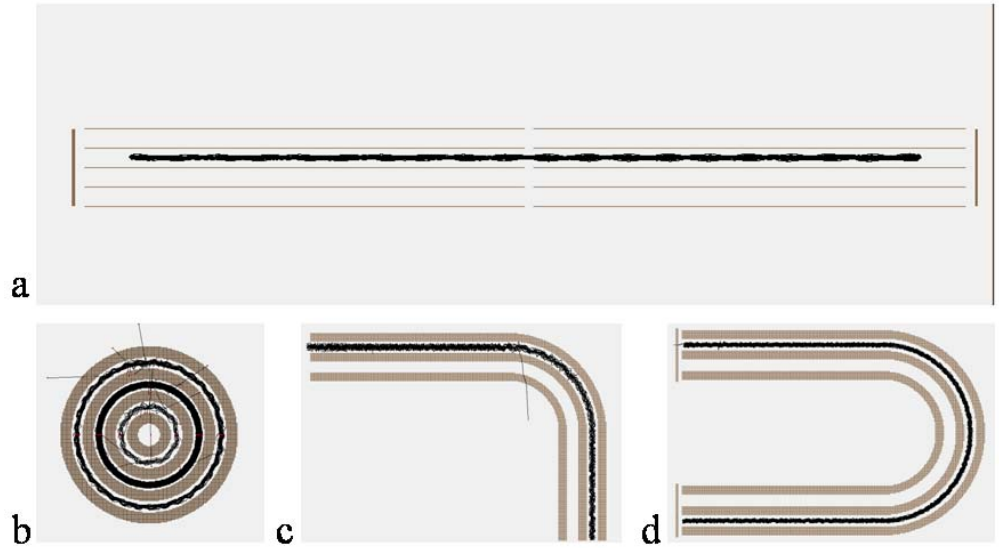


Figure 5. Geometries for surface electrode-type linear traps modeled in SIMION. (a) An array of straight surface electrodes with DC end caps on both sides. The electrons were trapped between RF biased surface electrodes radially and by the DC end caps axially. Electrons were trapped for a few milliseconds. (b) A circular surface electrode trap where electrons were trapped in concentric circular paths of various radii at the same time. (c) Geometry with a 90° turn to determine if the electron is trapped in a curvature. (d) A U-turn geometry where the electron was made to turn 180 degrees around the curvature.

FINANCIAL STATUS

R&D Status Report

Program Financial Status

15 July 2009 through 29 August 2009

Contract Item No.	Planned Expenses	Actual Expenses	% Budget Complete
0001	$101,568	102,562	6%
Project Commitments		9,260	
Total		$111,822	

Based on currently authorized work:

Is current funding sufficient for the current fiscal year (FY)? (Explain if NO) **Yes**

What is the next FY funding requirement at current anticipated levels **N/A (base fully funded)**

Have you included in the report narrative any explanation of the above data and are they cross referenced? **Yes**